REMARKS

Applicant has reviewed the Office Action dated December 16, 2008, and the references cited therein. **Claims 1-3 and 5-13** were previously pending and all have been rejected as obvious over the prior art. Applicant has amended the claims to more clearly distinguish Applicant's invention from the prior art cited in the Office Action.

In particular, Applicant amended claims 1 and 8 to clarify the differences between the claimed invention and the teachings of the prior art. Claims 1 and 8 have been amended, in accordance with the examples of programmed operation sequences provided on page 8, line 22 to page 12, line 27, to recite that dynamically controlling the writing of result data into the register file is carried out *without performing a jump operation.* Karp, in contrast to the claimed invention, relies upon branching (conditional jumping) to an exception handling routine to dynamically control writing of result data into the register file.

Applicant amended claims 2 and 9, pursuant to the disclosure at page 6, lines 7-11 of Applicant's original specification, to more particularly recite that the first identifier ("operation valid" index signal) indicates that the operation is invalid when the operation is a "NOP" operation. This additional clarification also distinguishes the claimed invention from the disclosure of Karp and the other cited references.

In view of the amendments, Applicant submits that the presently pending claims are patentable over the presently known prior art. Accordingly, Applicant requests favorable reconsideration of the previous objections and rejections in view of Applicant's amendments.

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Summary of The Prior Art-Based Claim Rejections

The following identifies the authority and prior art applied to the identified claims for each rejection of the claims set forth in the Office Action.

1. Claims 1-3, 5-6 and 8-12 are rejected under 35 U.S.C. §102(b) as being unpatentable over Karp U.S. Pat. No. 5,748,936 (Karp), in view of Kogge, "The Microprogramming of Pipelined Processors," 1981.

2. Claim 7 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Karp in view of Kogge and further in view of the Examiner's taking of Official Notice.

Applicant traverses each of the grounds for the rejection of the presently pending claims for the reasons set forth herein below.

Reasons for Traversing the Current Rejections of the Claims

Applicant traverses the rejection of claims 1-3, 5-6 and 8-12 as being obvious over Karp in view of Kogge since the invention recited in the independent claims (1 and 8) is not rendered by the combined teachings of these references. Applicant respectfully submits that the presently claimed invention recites a way of carrying out conditional writes to register files that is neither taught nor suggested by Karp. The claimed processor maintains sequential processing (no jump operations) while affecting conditional writes to the register files. In contrast, Karp discloses conditional writing by jumping to an exception handling routine.

The Cited Karp Reference

Karp, upon which the Final Office Action primarily relies, aims to improve the degree of instruction level parallelism at a VLIW processor by speculative execution of conditional operations. Karp discloses a system wherein during speculative execution of conditional operations, exceptions may occur that should be taken into account if the condition for the conditional operation turns out to be true. If the condition turns out to be false, the exception should be ignored. To that end Karp provides for a speculative look aside table (SLAT) 80 wherein a poison bit indicates whether an exception has occurred, and the SLAT is accessed via a predicate file 50. As shown in FIG. 5, the conditional writing is carried out through a branching operation and resulting exception handling.

Summary of the Presently Claimed Invention

In contrast to Karp's speculative execution, exception detection and poison bit handling routine arrangement, Applicant's claimed invention does not rely upon conditional branching to alternative program code. Rather, as explained through Applicant's examples, the conditional writes are carried out through sequentially executed programmed operations and the disclosed instruction logic arrangement schematically depicted, by way of two distinct examples, in FIGs. 1 and 2.

Karp Does Not Disclose Applicant's Claimed "Conditional Write Without Jump"

Applicant's claimed dynamically controlling write operations without performing a jump operation is neither disclosed nor suggested by Karp. Instead of Applicant's conditional write functionality that relies upon generating a dynamic write enable control signal in association with execution of a program instruction that potentially renders a writeable value, Karp discloses branching to an exception handling routine when an exception is generated and subsequently setting a "poison bit".

In a processor incorporating *Applicant's claimed invention*, a programmer dictates, via a *programmable criterion* embedded within a program code sequence, conditions under which a valid output has been rendered by one of the execution units. In the processor disclosed in Karp, there is a fixed/predetermined (i.e., non-programmable) set of conditions, usually defined by the machine architecture, that result in an exception and thereafter a conditional branch to an exception handling routine for setting of the poison bit. This essential difference is clarified in claims 1 and 8 by Applicant's most recent amendment.

The Prior Art References Do Not Disclose Applicant's Claimed "First Identifier"

Furthermore, Applicant submits that the invention recited in dependent **claims 2 and 9** is not disclosed in the combined teachings of the cited prior art references. In the processor according to an embodiment of the present invention, an unnecessarily large code-size is avoided by indicating a NOP operation by single bits in a header attached to the front of the VLIW instruction. In the illustrative embodiment of the invention recited in claims 2 and 9, *a first identifier* is used to indicate the presence of a NOP and therewith to disable the writing back of result data. The use of the NOP operation to indicate an invalid operation, incorporated into the recited elements of claims 2 and 9, is by no means disclosed by Karp. In
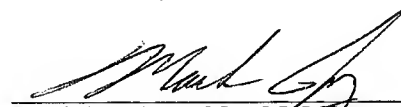
fact Karp points away from this measure. Karp, at col. 10, lines 16-21, states that the predicate may not be known until later because it is being computed as the current operation proceeds through the pipeline process. In contrast, in the processor according to the present invention the first identifier is known from the outset of instruction decoding, but it is delayed.

Thus, in summary, the invention recited in presently pending independent claims 1 and 8 (and dependent claims 2 and 9) provides a novel and inventive way to enable *programmable* conditional dynamic write operations in a time-stationary processor. The claimed invention enables custom operations to be executed by the execution unit that potentially produce more than one valid output without relying upon jump operations to achieve the conditional write functionality.

The rejections of each of the presently pending *dependent claims* have been overcome by Applicant's current amendments to the independent claims. Applicant reserves the right to address the basis for the rejection of the dependent claims, if needed, at a later time in response to any further rejection of independent claims 1 and 8.

Applicants respectfully submit that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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